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NUMERICAL ALGORITHMS AND PARALLEL TASKING(U)
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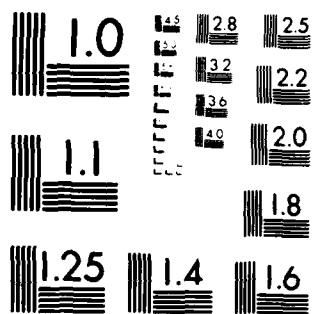
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31 ABSTRACT (Continue on reverse if necessary and identify by block number) During this research period progress has been made on the system integration of the software tasker to support algorithmic and applications segmentation for concurrent computing. This permits an efficient distribution of code and data on processing elements. The tasker provides primitives to support the segmenting of processes, monitors execution on worker processors by the manager on each concurrent system, and achieves asynchronous communication among worker processors and between the manager processor and the workers. Several technical presentations at scientific conferences were made during the research period, and one paper was submitted for publication.		DTIC ELECTRIC AUG 30 1984	
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AFOSR

Progress Report, AFOSR reference number 82-0210, "Numerical Algorithms and Parallel Tasking," Principal Investigator, Virginia Klema, Research Staff, George Cybenko and Elizabeth Ducot.

During the period, May 15, 1983 through May 14, 1984, Virginia Klema and Elizabeth Ducot have been supported for four months, and George Cybenko has been supported for one month. During this time system integration progress on the software tasker to support algorithmic segmentation and applications segmentation for concurrent computing permits locating of code and data on processing elements. The tasker provides primitives to support the segmenting of processes, monitors execution on Worker processors by the Manager on each concurrent system, and achieves asynchronous communication among Worker processors and between the Manager processor and the Workers.

Each workstation is a Multiple Instruction Multiple Data computing system in which the processing elements are Intel 86/30 boards with the 8086 central processing unit and the 8087 numeric data processor with IEEE floating point arithmetic in hardware. The 8087 is the key element in each processor. Each 86/30 Worker has 64K bytes of ROM and 256K bytes of configurable, private or dual ported, RAM. By deliberate intent the segmentation of algorithms or applications is the responsibility of the user.

Virginia Klema and Elizabeth Ducot presented a description of the concurrent computing environment at the SIAM Conference on Parallel Processing in Norfolk in November. Virginia Klema presented a talk with emphasis on IEEE floating point arithmetic and its applications at the SIGNUM Conference on Microprocessors in March. Virginia Klema also presented a description of the hardware and software environment for concurrency at the Workshop on Algorithms and Architectures at Kirtland Air Force Base in April. She will present a discussion of jack knife and bootstrap applications for concurrent tasking at the SIAM National Meeting in Seattle in July. George Cybenko submitted "Numerical Stability of the Lattice Algorithm for Least Squares Linear Prediction Problems" to BIT.

A copy of the PROGRAM SUMMARY sent to Dr. David Fox, June, 1984 is included with this progress report.

84 08 29 045

PROGRAM SUMMARY

"Numerical Algorithms and Parallel Tasking"

AFOSR-82-021

Principal Investigator, Virginia Klema
Massachusetts Institute of Technology

The long term goals are research on concurrent computing with emphasis on numerical algorithms for applications in signal processing and image processing. Data assembly, model fitting, and structured numerical optimization are common to both applications. The shorter term more specific goals are refinement and enhancement of the concurrent computing environment itself and the numerical algorithms that form the foundation for the applications.

Our concurrent computing environment is a Multiple Instruction Multiple Data (MIMD) configurable hardware system for experimental research. It is an Intel microprocessor based 86/30 board system with private and dual ported configurable memory, an 8086 central processing unit, and an 8087 numeric data processor on each processing element. The key component is the 8087, a chip with the IEEE binary standard (Draft 5, P754) for floating point arithmetic in hardware.

Design and implementation of a software tasker to locate code and data on Worker processors, monitor execution, and provide asynchronous communication among Worker processors and the Manager processor in each workstation is one specific topic of present research. Six Workers and a Manager can be in each workstation. Clusters of workstations are connected to each other through a VAX 11/730 that functions also as a file server. The VAX can monitor the performance of each workstation.

Basic modules for scientific computation for optimal and concurrent computing in an IEEE floating point arithmetic environment are designed and are being tested. These modules include, but are not limited to, matrix factorizations for linear systems and least squares problems, eigen and singular value decompositions, and their updates required for real-time computing.

Our concurrent environment is unique in that it is a dynamic system. By deliberate intent, the segmenting of modules for computation and the degree of concurrency requested is the responsibility of the user. The software tasker provides primitives to support assignment of concurrency within the algorithm or the application. New algorithmic approaches are needed for concurrent computing; our concurrent environment, hardware and software supports this research.

A principal challenge for our research is the melding of numerical analysis, algorithmic design for concurrency, specific applications, and analysis of concurrency. A favorable prospect for our research is the graceful migration of the basic computational modules and primitives for the software tasker to large scale MIMD machines.



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